AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 1 and 3 as follows:

LISTING OF CLAIMS:

1. (Currently Amended) A serial-data-communication apparatus for transmitting and receiving serial data composed of a plurality of bits including a start bit at a head, comprising:

edge-detection means for detecting a trailing edge of received data;

start-bit-level-inspection means for recognizing the reception of the start bit of said received data [[with]] based upon the detection of said trailing edge provided by said edge-detection means, and for monitoring a bit level of the start bit to examine whether the start bit maintains a predetermined bit level; and

start-bit-detection-error-notification means which outputs a signal to an external circuit, said signal indicating occurrence of an error in detecting the start bit, when any change in the bit level of the start bit is detected by said start-bit-level-inspection means.

2. (Original) The serial-data-communication apparatus according to claim 1, wherein said start-bit-detection-error-notification means outputs a signal, indicating occurrence of a start bit detection error, to a CPU, controlling the transmission and reception of the serial data, as an interrupt request signal.

3. (Currently Amended) A method of detecting a communication error in transmission and reception of serial data composed of a plurality of bits including a start bit at a head, comprising the steps of:

detecting a trailing edge of received data;

recognizing the reception of the start bit of said received data [[with]] based upon the detection of said trailing edge and, monitoring a bit level of the start bit to examine whether the start bit maintains a predetermined bit level; and

outputting a signal to an external circuit, the signal indicating occurrence of an error in detecting the start bit, when any change in the bit level of the start bit is detected.

4. (Original) The method of detecting a communication error according to claim 3, wherein the signal indicating occurrence of the error in detecting the start bit is output to a CPU, controlling the transmission and reception of the serial data, as an interrupt request signal.